specified row of memory locations and processing of the retrieved data to generate graphic signals;

memory control means;

a memory data bus having m lines and interconnecting the memory means and the memory control means to transmit m bits of data in parallel therebetween, where m is an integer; and

a processor data bus having n lines and interconnecting the data processing means and the memory control means to transmit n bits of data in parallel therebetween, where n is an integer and n>m;

said memory control means including storage means for temporarily storing successive groups of m bits of data [received serially on said memory data bus] read out from said memory means via said memory data bus by performing plural read operations within a memory cycle from memory locations at different column addresses of [the] said memory means at a row corresponding with the specified row address forming n bits of data by combining said successive groups of m bits of data, and transmitting said n bits of [the temporarily stored] data in parallel on said processor data bus to said data processing means for processing thereof to generate graphic signals.

2. (amended) A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding

column addresses, and rows, having corresponding row addresses, for storing data;

data processing means for specifying a row address in said memory means for writing of data in the memory locations at the different column addresses within the specified row of memory locations;

memory control means;

a memory data bus having m lines and interconnecting the memory means and the memory control means to transmit m bits of data in parallel therebetween, where m is an integer; and

a processor data bus having n lines and interconnecting the data processing means and the memory control means to transmit n bits of data in parallel therebetween, where n is an integer and n>m;

said memory control means including multiplexer means for multiplexing n bits of data received in parallel on said processor data bus into [serial] successive groups of m bits of data and applying [the serial] said successive groups of m bits of data to said memory data bus [for writing thereof] by performing plural write operations within a memory cycle in memory locations at different column addresses of the memory means at a row corresponding with the specified row address.

3. (amended) A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding column addresses, and rows, having corresponding row addresses, for storing data;

data processing means for specifying a row address of memory locations in said memory means for transfer of a data word therewith;

memory control means;

a memory data bus having m lines and interconnecting the memory means and the memory control means to transmit m bits of data in parallel therebetween, where m is an integer; and

a processor data bus having n lines and interconnecting the data processing means and the memory control means to transmit n bits of data in parallel therebetween, where n is a multiple of m;

said memory control means including counter means, responsive to receipt on said processor data bus of a row address specified by said processor means to specify an n-bit data word in said memory means, for successively generating n column addresses, applying the received row address and m of the generated column addresses on said memory data bus to transfer m bits of data between said memory means and said data processor means, with the data transfer including transfer of successive groups of m bits of data [in parallel] between said memory means and said memory control means by performing plural read/write operations within a memory cycle in said memory means, and

transfer of n bits of data between said memory control means and said data processor means by combining said successive groups of m bits of data to form said n bits of data.

4. (amended) A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding column addresses, and rows, having corresponding row addresses, for storing pixel information;

data processing means for specifying addresses of memory locations in said memory means for retrieval of pixel information therefrom and processing of the retrieved pixel information to generate graphic signals;

memory control means coupled to said memory means and [an] said data processing means for retrieving pixel information from said memory means in response to a request to retrieve pixel information from said data processing means at the specified address, [and] applying the retrieved pixel information to said data processing means for processing thereof, receiving processed pixel information from said data processing means, and storing processed pixel information in said memory means; and

output means connected to said memory control means for outputting processed pixel information to generate graphics.

8. (amended) A graphic processing apparatus comprising:

memory means, including a plurality of memory locations in an array of columns, having corresponding column addresses, and rows, having corresponding row addresses, for storing data;

data processing means for specifying a row address in said memory means for transfer of data between the data processing means and the memory locations at the different column addresses within the specified row of memory locations;

memory control means;

a memory data bus having m lines and interconnecting the memory means and the memory control means to transmit m bits of data in parallel therebetween where m is an integer; and

a processor data bus having n lines and interconnecting the data processing means and the memory control means to transmit n bits of data in parallel therebetween, where n is an integer and n>m;

said memory control means including storage means for temporarily storing successive groups of m bits of data [received on said memory bus] read out from said memory means via said memory data bus by performing plural read operations within a memory cycle from memory locations at different column addresses of [the memory locations] a row of said memory means corresponding to [with] the specified row address, forming m bits of data by combining said

successive groups of said m bits of data, and transmitting said n bits of [the temporarily stored] data in parallel on said processor data bus to said data processing means for processing thereof, and multiplexer means for multiplexing n bits of data received in parallel on said processor data bus into [serial] successive groups of m bits of data and applying said successive groups of m bits of [the serial] data to said [serial] memory data bus [for writing thereof] by performing plural write operations within a memory cycle in memory locations at different column addresses of the [memory location] row corresponding [with] to the specified row address.

9. (amended) A graphic processing apparatus comprising:

memory means for storing graphic data;

data processing means for executing a predetermined processing on graphic data read out from said memory means;

memory control means for controlling transference of graphic data stored in said memory means to said data processing means in accordance with a request from said data processing means;

a first bus having m lines and interconnecting said memory means and said memory control means to transfer m bits of data in parallel therebetween, where m is an integer; and

a second bus having n lines and interconnecting said data processing means and said memory control means to transfer n bits of data in parallel therebetween, where n is an integer and n>m;

wherein said memory control means includes storage means for temporarily storing successive groups of n bits of data read out from said memory means via said first bus by performing plural read operations within a memory cycle, said memory control means forms n bits of data by combining said successive groups of m bits of data and transfers said n bits of data in parallel to said data processing means via said second bus.

10. (amended) A graphic processing apparatus comprising:

memory means for storing graphic data;

data processing means for executing a predetermined processing to generate graphic data;

memory control means for controlling transference of graphic data generated by said data processing means to said memory means in accordance with a request from said data processing means;

a first bus having m lines and interconnecting said memory means and said memory control means to transfer m bits of data in parallel therebetween, where m is an integer; and

a second bus having n lines and interconnecting said data processing means and said memory control means to

transfer n bits of data in parallel therebetween, where n is an integer and n>m;

wherein said memory control means includes multiplexing means for multiplexing n bits of data received in parallel via said second bus from said data processing means into successive groups of m bits of data, said memory control means transfers said successive groups of m bits of data to said memory means via said first bus by performing plural write operations within a memory cycle.

11. (amended) A graphic processing apparatus comprising:

memory means, having m bit terminals, for storing graphic data, said graphic data being read out in successive groups of m bits of data from the memory means, where m is an integer;

data processing means, having n bit terminals, for executing a predetermined processing on n bits of data read out from said memory means, said n bits of data being supplied to said data processing means in parallel, where n is an integer and n>m;

interface means, having m bit terminals coupled to said memory means and n bit terminals coupled to said data processing means, for transferring graphic data stored in said memory means to said data processing means in accordance with a request from said data processing means;

wherein said interface means includes converting means for converting said successive groups of m bits of

data, read out from said memory means by performing plural read operations within a memory cycle, into said n bits of data to be supplied in parallel to said data processing means.

12. (amended) A graphic processing apparatus comprising:

memory means, having m bit terminals, for storing graphic data, said graphic data being written sequentially as successive groups of m bits of data into said memory means, where m is an integer;

data processing means, having n bit terminals, for executing a predetermined processing to generate graphic data, said generated graphic data being transferred in parallel as n bits of as data, where n is an integer and n>m;

interface means, having m bit terminals coupled to said memory means and n bit terminals coupled to said data processing means, for transferring graphic data generated by said data processing means to said memory means in accordance with a request from said data processing means;

wherein said interface means includes converting means for dividing said n bits of data from said data processing means into successive groups of m bits of data to be transferred to said memory means by performing plural write operations within a memory cycle.

14. (amended) A graphic processing apparatus according to claim 9 wherein said successive groups of m bits of data to be converted are read out of said memory means by performing plural read operations within a memory cycle based on an address specified by said data processing means.

16. (amended) A graphic processing apparatus according to claim 9 wherein said successive groups of m bits of data each include an m bit portion of said n bits of data.

18. (amended) A graphic apparatus according to claim 11 wherein said successive groups of m bits of data to be converted are read out of said memory means by performing plural read operations within a memory cycle based on an address of specified by said data processing means.

19. (amended) A graphic processing apparatus according to claim 11 wherein said n bits of data converted from said successive groups of m bits of data read out from said memory means by performing plural read operations within a memory cycle is applied to said data processing means in a unit of time more than two times said memory cycle.

20. (amended) A graphic processing apparatus according to claim 11 wherein said successive groups of m bits of data each includes an m bit portion of said n bits of data.

21. (amended) A memory read method for reading data from a memory in accordance with a request from a processor, comprising the steps of:

reading out successive groups of m bits of data from said memory through an m-bit bus by performing plural read operations within a memory cycle, each group of m bits of data being read out based on an address specified by said processor, where m is an integer;

converting said successive groups of m bits of data into n bits of data by combining said successive groups of m bits of data, where n is an integer and n>m; and

applying said n bits of data in parallel to said processor through an n-bit bus.

22. (amended) A memory write method for writing data generated in a processor into a memory in accordance with a request from said processor, comprising the steps of:

receiving n bits of data in parallel from said processor through an n-bit bus, where n is an integer;

converting said received n bits of parallel data into successive groups of m bits of data by dividing said n bits of data, where m is an integer and n>m; and

writing said converted m bits of successive groups of data into said memory through an m-bit bus by performing plural write operations within a memory cycle based on an address specified by said processor.

23. (amended) A memory controller for controlling transference of data between a memory and a processor, said memory controller comprising:

m bit terminals for coupling to said memory, wherein successive groups of m bits of data is transferred through said m bit terminals between said memory and said controller by performing plural read operations within a memory cycle, where m is an integer;

n bit terminals for coupling to said processor, wherein n bits of data is transferred in parallel through said n bit terminals between said controller and said processor, where n is an integer and n>m; and

converting means for making a conversion between n bits of data from said n bit terminals and successive groups of m bits of data from said m bit terminals corresponding thereto by combining said successive groups of m bits of data to form said n bits of data and dividing said n bits of data to form said successive groups of m bits of data.

24. (amended) A memory controller according to claim 23 wherein said successive groups of m bits of data from said m bit terminals to be converted are read out of said memory by performing plural read operations within a memory cycle based on an address specified by said processor.

25. (amended) A memory controller according to claim 24 wherein said n bits of data from said n bit terminals to

be converted is applied to said processor in a unit of time more than two times said memory cycle.

26. (amended) A memory controller according to claim 23 wherein said successive groups of m bits of data each includes an m bit portion of said n bits of data.

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28. (amended) A memory read method for reading data from a memory in accordance with a request from a processor, comprising the steps of:

reading out successive groups of data from said memory by performing plural read operations within a memory cycle based on an address specified by said processor;

converting said read out successive groups of data into parallel data by combining said successive groups of data; and

applying said converted parallel data to said processor in a unit of time more than two times said memory cycle.

29. (amended) A memory read method according to claim 28 wherein each of said successive groups of data, read out from said memory by performing plural read operations within a memory cycle, forms a portion of said parallel data to be applied to said processor.

30. (amended) A memory read method according to claim 28 wherein each of said successive groups of data, read out

from said memory by performing plural read operations within a memory cycle, is composed of m bits of data, said parallel data applied to said memory is composed of n bits of data and wherein both n and m are integers and n>m.

32. (amended) A memory write method for writing data generated by a processor into a memory in accordance with a request from said processor, comprising the steps of:

receiving data in parallel from said processor within a predetermined unit of time;

converting said received parallel data into successive groups of data each having a portion of said received parallel data; and

writing said converted successive groups of data into said memory by performing plural write operations within a memory cycle based on an address specified by said processor, wherein said memory cycle is less than one half said predetermined unit of time.

33. (amended) A memory write method according to claim 32 wherein said parallel data received from said processor is composed of n bits of data and each of said converted successive groups of data, to be written into said memory by performing plural write operations within a memory cycle, is composed of m bits of data where m and n are both integers and n>m.

44. (amended) A graphic processing apparatus comprising:

a memory for storing graphic data;

a data processor for executing a predetermined graphic processing to generate graphic data to be stored in said memory;

output means for outputting said graphic data read out from said memory;

a memory controller for controlling data transfer between said memory and said data processor in accordance with a request from said data processor;

a first bus, having m (wherein m is an integer) bits width, connected between said memory and said memory controller, for transferring m bits of data in parallel; and

a second bus, having n (wherein n is an integer, n > m) bits width, connected between said memory controller and said data processor, for transferring n bits of data in parallel;

wherein said memory controller comprises:

a storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said first bus,

means for forming n bits of data using said successive groups of m bits of data and supplying said n bits of data in parallel to said data processor through said second bus, and

a converter for converting said graphic data temporarily stored in said memory into serial data which is provided to said output means.

45. (amended) An apparatus according to claim 44, wherein said memory controller further comprises:

a multiplexer for outputting said n bits of data transferred from said data processor to said first bus having m bits width in successive groups of m bits of data during said predetermined period of time.

46. (amended) An apparatus according to claim 44, wherein said memory controller further comprises:

means for generating an address signal for accessing said memory plural times, in response to a signal for accessing said memory supplied from said data processor, to obtain successive groups of m bits of data.

47. (amended) An apparatus according to claim 44, wherein said successive groups of m bits of data to be transferred to said memory controller through said first bus is read out by accessing said memory plural times within a unit transfer time based on an access signal to said memory designated by said data processor.

48. (amended) An apparatus according to claim 47, wherein said successive groups of m bits of data transferred to said memory controller through said first bus is combined